REMARKS

Claims 1-9 and 27-30 are pending. Claims 10-26 were previously withdrawn. No new matter has been added.

Claims 1-6 are rejected as being unpatentable over the combination of Lum (U.S. Patent No. 5,696,931, hereinafter "Lum") in view of Hicken (U.S. Patent No. 6,092,149, hereinafter "Hicken"), Napolitano (U.S. Patent No. 6,301,605, hereinafter "Napolitano"), and Shinagawa (U.S. Patent No. 5,937,427, hereinafter "Shinagawa"). Applicant respectfully traverses the section 103(a) rejection because Lum, Hicken, Napolitano, and Shinagawa do not teach or suggest all of the limitations of the claims as currently provided.

Claim 1 requires that "the request of the transfer (of the requested data that resides in the mass storage device) and the initiation of the auto-transfer (of the requested data that resides in the cache) occurs substantially concurrently." The Examiner, in the Office Action dated November 14, 2008, has conceded that Lum, Hicken, and Napolitano do not explicitly disclose the request of the transfer (i.e., from mass storage device to host) and the initiation of the auto-transfer (i.e., from cache to host) occurs substantially concurrently (see Office Action paragraph on page 5). Examiner has asserted, however, that Shinagawa discloses request of a transfer (i.e., from mass storage device to host) and initiation of a transfer (i.e., from cache to host) occurs substantially concurrently. Applicant respectfully traverses that assertion.

Shinagawa discloses in column 1, lines 28-37 that "As a write method using a cache memory, several methods such as a write-through method, a write-back method, and the like are known. In the write-through method, when a certain file (data) is written to a disc...the file is

stored in a cache memory, and is simultaneously written to the disc." Rather than concurrently transferring data from the mass storage device to the host and from the cache to the host as required in Claim 1, Shinagawa discloses simultaneously transferring the file (data) from host to the cache memory and to the disc. Additionally, Shinagawa discloses in column 4, lines 25-29 that "The ODC 9 has...a function of simultaneously executing data transfer between the interface 3 and the cache memory 7 and data transfer between the cache memory 7 and the R/W control unit 4 in response to the command." Neither of these teachings by Shinagawa, however, discloses the substantially concurrent transfer of requested data from mass storage device to host and from cache to host.

Furthermore, the requested data residing in the mass storage device and the requested data residing in the cache are different data comprising a portion of the requested data that resides in the mass storage device and a portion of the requested data that resides in the cache, whereas Shinagawa discloses that the same file (data) is written to the cache memory and to the disc.

Accordingly, Applicant submits that Claim 1 is patentable over Lum, Hicken, Napolitano, and Shinagawa and respectfully request withdrawal of the Examiner's rejection.

Claims 2-6 depend from Claim 1. Applicant respectfully submits that these dependent claims are patentable over the cited prior art, not only because of their dependency from Claim 1 for the reasons discussed above, but also in view of their novel claim features.

Claims 8, 27-28, and 30 were rejected as being unpatentable over the combination of Lum over Simionescu (U.S. Patent No. 6,141,728, hereinafter "Simionescu") in view of Napolitano and Shinagawa. Applicant respectfully traverses the section 103(a) rejection because

Lum, Simionescu, Napolitano, and Shinagawa do not teach or suggest all of the limitations of the claims as currently provided.

Claim 8 requires that "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system substantially concurrently with transferring the portion of the requested data from the mass storage device directly to the host system." Claims 27-28 require "to concurrently cause said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request from said disk-device." Examiner, in the Office Action dated November 14, 2008, has conceded that Lum, Simionescu, and Napolitano do not explicitly disclose the request of the transfer (i.e., from mass storage to host) and the initiation of the auto-transfer (i.e., from cache to host) occurs substantially concurrently. Examiner has asserted, however, that Shinagawa discloses request of a transfer (i.e., from mass storage device to host) and initiation of a transfer (i.e., from cache to host) occurs substantially concurrently. Applicant respectfully traverses that assertion.

Shinagawa discloses in column 1, lines 28-37 that "As a write method using a cache memory, several methods such as a write-through method, a write-back method, and the like are known. In the write-through method, when a certain file (data) is written to a disc...the file is stored in a cache memory, and is simultaneously written to the disc." Rather than transferring data from the mass storage device to the host and from the cache to the host as required in Claim 8, Shinagawa discloses transferring the file (data) from host to the cache memory and to the disc. Furthermore, the requested data residing in the mass storage device and the requested data

residing in the cache are different data, whereas Shinagawa discloses that the same file (data) is written to the cache memory and to the disc.

Accordingly, Applicant submits that Claim 8 and Claim 27-28 are patentable over Lum, Simionescu, Napolitano, and Shinagawa, and respectfully request withdrawal of the Examiner's rejection.

Claims 30 depends from claim 28. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from Claim 28 for the reasons discussed above, but also in view of its additional novel claim features.

Claim 7, which depends from claim 1, was rejected as being unpatentable over the combination of Lum in view of Hicken, Napolitano, Shinagawa, and well-known practices in the art, with Examiner asserting that "integrating memory and logic on a single device is a common and well-known practice in the art." However, Examiner has identified no well-known practices in the art that teach or suggest "the request of the transfer (of the requested data that resides in the mass storage device) and the initiation of the auto-transfer (of the requested data that resides in the cache) occurs substantially concurrently," as recited in claim 7 by dependence from claim 1. Hence, the asserted well-known practices in the art, taken alone or in combination, fail to overcome the deficiencies in the combination of Lum, Hicken, Napolitano, and Shinagawa discussed above with regard to claim 1. Applicant respectfully submits that dependent claim 7 is patentable over the cited prior art, not only because of its dependency from claim 1 for the reasons discussed above, but also in view of its additional novel claim features.

Claim 29 was rejected as being unpatentable over the combination of Lum in view of Simionescu, Napolitano, Shinagawa and well-known practices in the art, with Examiner asserting that "integrating memory and logic on a single device is a common and well-known practice in the art." However, Examiner has identified no well-known practices in the art that teach or suggest, "to concurrently cause said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device," as required in claim 29 by dependence from claim 28. Hence, the asserted well-known practices alone or in combination fail to overcome the deficiencies in Lum, Simionescu, Napolitano, Shinagawa discussed above with reference to claim 28. Applicant respectfully submits that dependent claim 29 is patentable over the cited prior art, not only because of its dependency from claim 28 for the reasons discussed above, but also in view of its additional novel claim features.

Claim 9 was rejected as being unpatentable over the combination of Lum in view of Simionescu, Napolitano, Shinagawa, and U.S. Patent Publication No. 2001/0014929 to Taroda et al. (hereinafter "Taroda") with Examiner asserting that Taroda teaches "a disk control device having a block format different from the host wherein the first and second formats can be converted to realize access compatible with two different formats." Examiner has not identified any disclosure in Taroda that "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system substantially concurrently with transferring the portion of the requested data from the mass storage devices to the host system,"

as recited in claim 9 by dependence from claim 8. Hence, Taroda fails to overcome deficiencies, discussed above with regard to claim 8, of Lum, Simionescu, Napolitano, and Shinagawa, taken alone or in combination. Applicant respectfully submits that dependent claim 9 is patentable over the cited prior art, not only because of its dependency from claim 8 for the reasons discussed above, but also in view of its additional novel claim features.

Claim 1 was also rejected as being unpatentable over Lum in view of Hicken, Napolitano, and Satoh (U.S. Patent 5,313,612, hereinafter "Satoh"). Applicant respectfully traverses the section 103(a) rejection because Lum, Hicken, Napolitano, and Satoh do not teach or suggest all of the limitations of the claims as currently provided.

Claim 1 requires that "the request of the transfer (of the requested data that resides in the mass storage device) and the initiation of the auto-transfer (of the requested data that resided in the cache) occurs substantially concurrently." The Examiner, in the Office Action dated November 14, 2008, has conceded that Lum, Hicken, and Napolitano do not explicitly disclose the request of the transfer (i.e., from mass storage device to host) and the initiation of the auto-transfer (i.e., from cache to host) occurs substantially concurrently (see Office Action paragraph on page 5). Examiner has asserted, however, that Satoh discloses request of a transfer (i.e., from mass storage device to host) and initiation of a transfer (i.e., from cache to host) occurs substantially concurrently. Applicant respectfully traverses that assertion.

Satoh discloses in column 7, lines 60-66 that "said optical disk control means controls said disk cache memory to write said host data transmitted from said host device into said disk cache memory at the same time that said-updating control commands and said host data are written from said host device into said work optical disk drive." Rather than substantially

concurrently transferring data from the mass storage device to the host and from the cache to the host as required in Claim 1, Satoh discloses transferring the host data from host device to the cache memory and to the optical disk drive. Furthermore, the requested data residing in the mass storage device and the requested data residing in the cache are different data, whereas Satoh discloses that the same host data is written to the cache memory and to the optical disk drive.

Accordingly, Applicant submits that Claim 1 is patentable over Lum, Hicken, Napolitano, and Satoh and respectfully request withdrawal of the Examiner's rejection.

Claim 8 was also rejected as being unpatentable over Lum in view of Hicken, Napolitano, and Satoh. Applicant respectfully traverses the section 103(a) rejection because Lum, Hicken, Napolitano, and Satoh do not teach or suggest all of the limitations of the claims as currently provided.

Claim 8 requires that "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system substantially concurrently with transferring the portion of the requested data from the mass storage device directly to the host system." Examiner, in the Office Action dated November 14, 2008, has conceded that Lum, Simionescu, and Napolitano do not explicitly disclose the request of the transfer (i.e., from mass storage to host) and the initiation of the auto-transfer (i.e., from cache to host) occurs substantially concurrently. Examiner has asserted, however, that Satoh discloses request of a transfer (i.e., from mass storage device to host) and initiation of a transfer (i.e., from cache to host) occurs substantially concurrently. Applicant respectfully traverses that assertion.

Satoh discloses in column 7, lines 60-66 that "said optical disk control means controls said disk cache memory to write said host data transmitted from said host device into said disk cache memory at the same time that said-updating control commands and said host data are written from said host device into said work optical disk drive." Rather than substantially concurrently transferring data from the mass storage device to the host and from the cache to the host as required in Claim 1, Satoh discloses transferring the host data from host device to the cache memory and to the optical disk drive. Furthermore, the requested data residing in the mass storage device and the requested data residing in the cache are different data, whereas Satoh discloses that the same host data is written to the cache memory and to the optical disk drive.

Accordingly, Applicant submits that Claim 8 is patentable over Lum, Hicken, Napolitano, and Satoh and respectfully request withdrawal of the Examiner's rejection.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner please contact Applicant's attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

13 FEB 2009
Date

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